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David Sarnoff Research Center
Subsidiary of SRI International

CERAMIC/METAL COMPOSITE CIRCUIT-BOARD-LEVEL TECHNOLOGY FOR APPLICATION SPECIFIC ELECTRONIC MODULES (ASEMs)

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TECHNICAL REPORT

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Summary

- The Phase I program began January 3, 1994

- A limited number of electrical feedthroughs have been fabricated in 13 mil diameter holes in a 20 mil thick metal core, using screen printing techniques. This technique shows promise as a low cost, mass fabrication process for producing a large number of electrical feedthroughs. A glass (for the feedthrough insulator) has been found that exhibits good adhesion and wetting of the metal core surface. Furthermore, it is thought that these techniques can be extended to produce 50Ω interconnections (20 - 30 mil diameter).

- Several ceramic formulations have been developed this past quarter that exhibit excellent high frequency dielectric properties and have a CTE that is between Si and GaAs. These formulations show promise for use as the basis of the green tape that will form the LTCC-M structure.

- Several of the LTCC ceramics that have been developed show low dielectric loss ($0.001 < \tan\delta < 0.002$) in the 10 - 20GHz frequency range. Such ceramics are highly desirable for the construction of military T/R modules. Developing these ceramics into an LTCC-M process technology will show a path to the production of high volume, low cost T/R modules for military electronics.

Section I
WBS Task 1.1: Metal Core Fabrication

A. Task Objective

The development of a process to fabricate many small electrical feedthroughs within the metal core. These feedthroughs must be fabricated with a very high yield, low cost process that offers high reliability and compatibility with the LTCC-M process technology. Screen printing techniques tested this past quarter, show promise as a low cost fabrication process using established equipment.

B. Introduction

The development of a technology to fabricate many small electrical feedthroughs within the metal core is one of the central features of the Phase I research program. To obtain high reliability, the insulator in the hole must match the thermal expansion of the metal core (5/90/5 or 13/74/13 Cu/Mo/Cu clad laminate manufactured by Climax Specialty Metals). Phase I will begin by concentrating on the fabrication of 13 mil diameter electrical feedthroughs, the smallest standard plated-through hole used by the printed wiring board industry. For applications requiring 50Ω feedthroughs, a model of the feedthrough as a long transmission line indicates that the smallest holes will be 20 - 30 mils in diameter.

The basic feedthrough fabrication process involves opening up a hole (e.g. drilling and deburring), applying a layer of nickel to seal the molybdenum, depositing an annular ring of insulation, and finally depositing a conductor in the center core of the insulator. The conductor and insulator must be able to withstand several 900°C firing steps required to complete the LTCC-M fabrication process. For high module yields the insulator must be deposited above a minimum thickness and not contain pinholes. After the hole has been formed, the insulator can be deposited by either screen printing techniques or by electrophoretic deposition. Figure I.1 shows the general process steps required by these methods. During this past quarter, two screen printing processes and an electrophoretic deposition process were investigated, and will be described in this report. The screen printing techniques show promise for low cost fabrication of metal core feedthroughs.

C. Insulator Deposition by Screen Printing:

Thick film dielectric inks can be readily deposited into 13 mil diameter holes in 20 mil thick metal cores using screen printing, stencil or doctor blade techniques on standard screen printers. The major process control parameters are the rheology of the ink formulation and the strength of the vacuum that is pulling on the underside of the metal core during the printing operation. For a given ink formulation, a high vacuum can cause annular rings of thick film dielectric to form in the holes, while a low vacuum can lead to holes completely filled with dielectric material. The advantage of the high vacuum is that annular rings of insulating material are deposited as a group with a single process step. As shown in Figure I.1, the low vacuum process requires an additional sequential punching operation to form the annular rings. An important issue

that must be addressed is whether the high vacuum formation of annular rings is a sufficiently robust process to allow nearly 100% yields.

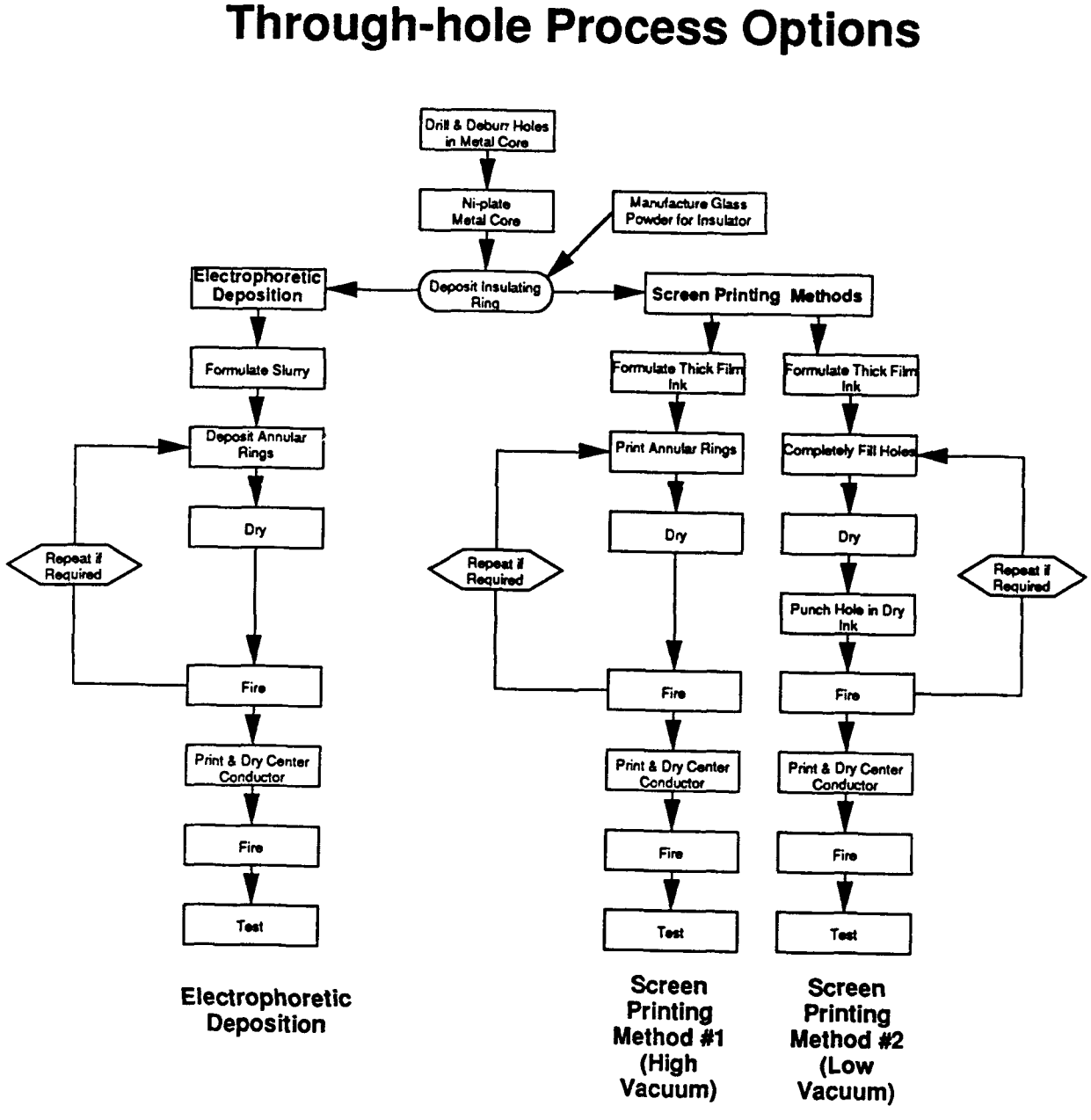


Figure I.1: Process steps for several options for ceramic insulator deposition into the metal core holes.

D. Insulator Deposition by Electrophoresis

A method particularly suited for depositing insulating powders is electrophoresis[1]. It relies on the relation between the hydrodynamic radius of a particle and its double layer radius. The former depends on particle size, the latter on the square root of the ionic strength of the liquid medium. Electrophoresis will occur when the hydrodynamic radius is less than the double layer radius. The process for deposition of glass powder on metal boards, including kinetics, has been presented in detail[2].

The charge necessary to create the double layer in some of the barium-magnesium-boro-silicate glasses is believed to be a reaction of the barium in the glass structure with water; the barium ions thus form the positively charged inner region of the double layer. Glasses may sometimes require adsorbed ionic surfactants to supply the charge.

There is no observed electrochemical reaction associated with the formation of the deposited material, the buildup being a result of impingement. In that sense, the process is similar to settling, but unlike settling, where the largest particles deposit first, the electrophoretic deposit has a distribution of particle size similar to that of the slurry (except for the particles which are excluded by double layer dimensions). The particle velocity is otherwise independent of size[3].

The laboratory process developed at Sarnoff relies on a deposition cell in which the glass slurry is pumped over baffles so as to flow symmetrically between the (negative) substrate at the mid-plane and the (positive) counter electrodes[4]. This produces two sheets of slurry whose particle concentration and size distribution remain substantially constant over the deposition area. Since the electric field is between plane-parallel electrodes, the deposition rate is uniform over both sides of the 2"x3" substrate. Either constant current (linear deposition with time) or constant voltage (easier instrumentation) may be employed.

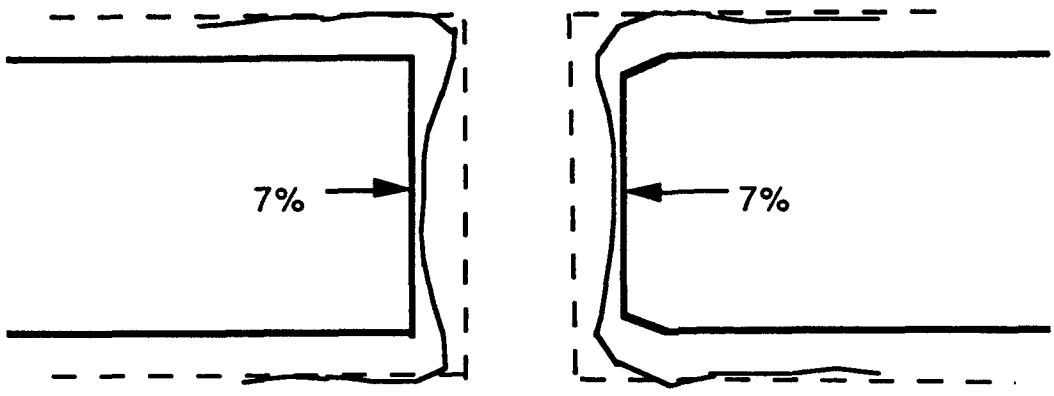
There are two difficulties encountered with the deposition of glass into the holes. First, as the diameter of the hole decreases, the shielding of the electric field by the cavity walls reduces the "reach" of the deposition field. This can be demonstrated by using a two-dimensional electrolytic tank with metal electrodes to measure the fields normal to the edges, which are proportional to the deposition currents. For example, for a 0.0135" hole diameter and 0.020" core thickness with unchamfered corners, a length-to-width ratio of 1.5, the field (and therefore the deposit) falls to 50% at a depth of 0.003", and to a minimum of about 14% at the center. In order to guarantee sufficient dielectric isolation, it is estimated that the minimum thickness of the fired insulator should be at least 0.001". Because of shrinkage during firing, a deposit thickness of 0.002" is required at the center minimum. This is unlikely to be achieved with a single deposition in an unchamfered hole, because depositing 0.001" of glass at the center could require as much as 0.007" at the top, likely to close the hole at both ends. Experimental verification of the fired deposit contour for a 0.0135" hole without chamfering are visible in the photograph of a cross-section, Figure I.2. The same considerations apply for electroplated nickel, but are not serious because the nickel plating is required to be only 0.0003" thick; enough nickel may be deposited at the hole center without affecting the hole ends. Alternatively, the nickel may be deposited by an electroless process.

Figure I.2: Fired ceramic that was electrophoretically deposited inside a metal core hole.

The electrolytic tank technique was used to design satisfactory chamfers for electrophoretic deposition into holes. By chamfering the holes, shielding of the electrostatic field at the hole center can be reduced, thus increasing the coating thickness at the hole center for a given coating thickness at the ends. Measurements of the normal field for cross-sections with different degrees of chamfering are shown in Figures I.3(a)-(d). The amount of deposited glass powder is expected to be proportional to the field. Figure I.3(a) shows the unchamfered hole, and I.3(b) shows a slightly chamfered hole . The field at the center of either hole is not significantly different, so a slight chamfer does affect the deposited contour very much. In Figures I.3(c) and I.3(d), a narrow thin chamfer shows significant influence on the deposit at the center of the hole. Starting with a chamfer between 1:4 and 2:4, the deposition would be expected to produce a uniform insulation of about 40% the thickness on the surface.

We anticipate masking the core board surface except for the chamfered area which will act as the base for the conductor pad. Tests using drilled Delrin and etched copper foil as shields are under way. Limited success has been achieved by doctor blading the board surface free of deposited powder.

A second consideration associated with filling insulating the holes is related to surface tension of the glass and its wetting characteristics (surface energy) with respect to the oxidized nickel surface. A glass has been chosen which exhibits good adhesion and wetting of the oxidized nickel surface.



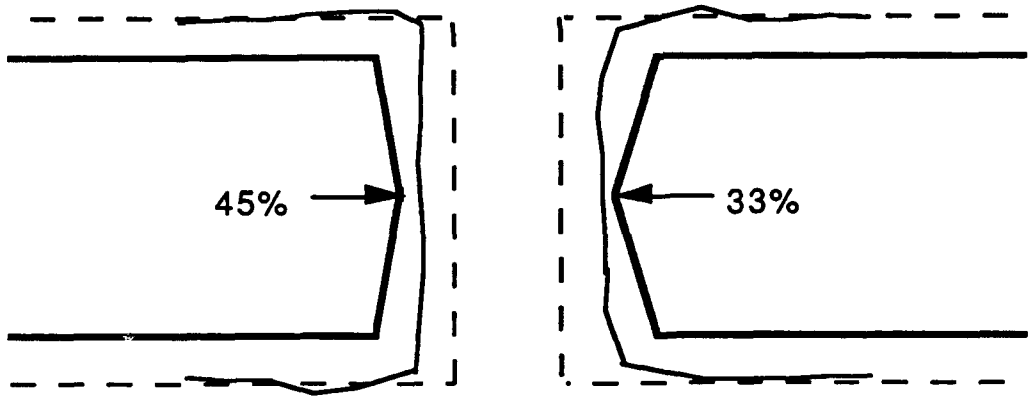


Figure 3: Measured electrostatic field for different degrees of hole chamfering.

E. Center Conductor Deposition

The central conductor can be deposited using standard screen printing or suction techniques. These conductors can be deposited as annular rings after the insulating ring has been fired, or they can completely fill the central region of the

through-hole. Annular ring conductors have been deposited using a thick film ink consisting of a silver resinate mixed in an ethyl cellulose organic vehicle. After firing at 640°C, these films were nickel/gold plated in electroless baths. If a completely filled central region is desired, then a thick film via ink can be deposited into the hole by stencil printing techniques.

F. Results to Date

Using a doctor blade technique, annular rings have been readily formed using a high vacuum pulling of the ink through a 13 mil diameter hole in a 20 mil thick metal core. A typical insulating ring (1 printing step) after the ceramic has been fired is shown in Figure I.4. The thick film ink formulation has not yet been optimized for this process. The ink is based on a crystallizing glass (forms willemite after firing) that is compatible with the coefficient of thermal expansion, CTE, of Mo, mixed in an appropriate organic vehicle. The dielectric thickness after 1 print and fire (820°C in air) cycle seems to be too thin, so two print and fire cycles are being tested. A cross section through the insulation of a twice printed and fired feedthrough is shown in Figure I.5. These insulating rings have been coated with a thick film conductor printed through a stencil (2 mil thick stainless steel) having 10 mil diameter openings. The conductor ink was a commercial Ag resinate mixed in an ethyl cellulose-based organic vehicle. After firing (640°C in air), this produced continuous conducting films within the holes that could be further (if required) plated up in electroless Ni and Au baths. This process has already produced acceptable electrical feedthroughs in a Copper/Stainless Steel #409/Copper metal core, such as the one shown in Figure I.6. Work is continuing to reduce the defects formed in the insulating rings, and to reduce the number holes where the dielectric ink completely fills the hole after printing. The latter problem is dependent on the individual metal core (and its flatness).

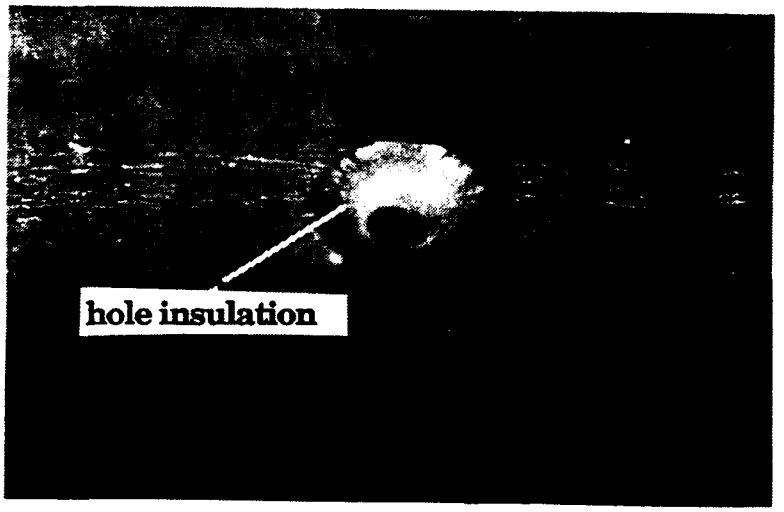


Figure I.4: Insulated metal through-hole (0.013 mil diameter) after 1 screen printing (i.e. doctor blade) step.

Insulated Through-hole in Metal Core

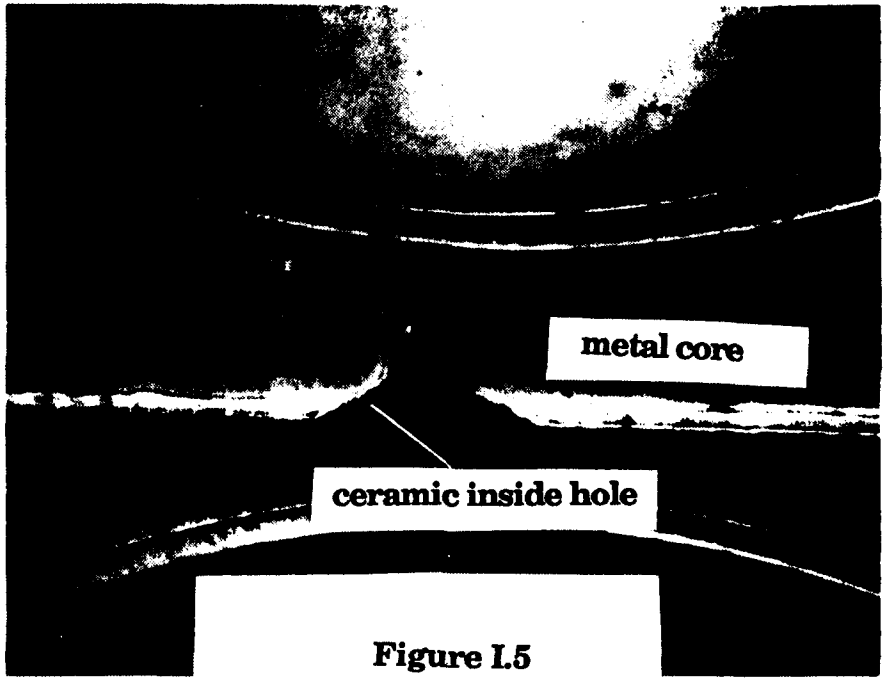


Figure I.5

Cross-section showing insulation in a 13 mil diameter through-hole in Cu/ SS#409/Cu. The insulation was deposited by screen printing techniques.

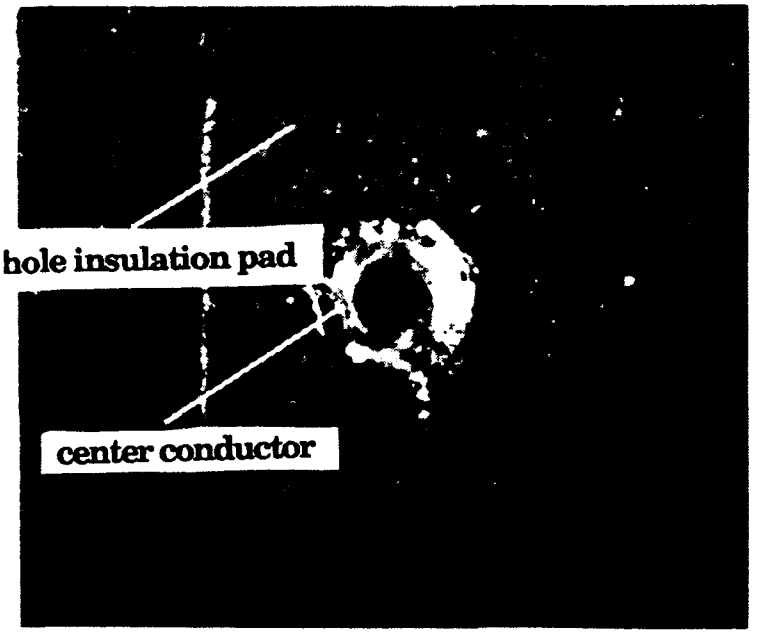


Figure I.6: A metal core through-hole (13 mil diameter, 20 mil thick metal core) produced entirely by low cost screen printing techniques

Using the same thick film ink and doctor blade technique, holes completely filled with dielectric can be made by pulling the ink through the metal core with a low vacuum. The dielectric center core must be removed with a small (e.g. 5 mil diameter) via punch. Tooling is currently being made to hold and register (±1 mil) the drilled metal core to the green tape via punch. After completion of the tooling, work will continue in the development of this process.

Electrophoretic depositions have been made using a high thermal expansion metal-glass system. The 0.030" holes show good insulation, but holes of 0.020" and 0.0135", when checked with the electrolytic probe, do not. This is a result of the shielding of the field in the holes. Experimental models using a two dimensional electrolytic tank confirm these results. The tank experiments show that a chamfer of about 15° - 20° will produce good insulator coverage, with insulation parallel to the hole axis.

A low expansion glass, compatible with the Cu/Mo/Cu boards exhibits good adhesion and compatibility with the oxidized nickel surface.

G. Important Findings and Conclusions

Electrical feedthroughs have been fabricated in 13 mil diameter holes in a metal core, using screen printing techniques. This technique shows promise as a low cost, mass fabrication process for producing a large number of electrical feedthroughs. A glass has been found that exhibits good adhesion and wetting of the oxidized nickel surface.

H. Plan for the Upcoming Quarter

- The screen printing techniques, which do not suffer from the shielding limitations of electrophoresis, will be emphasized during the upcoming

quarter. The techniques will be optimized for uniform coating of the insulating glass within the holes.

- Through-holes will be fabricated in Copper/Molybdenum/Copper cores instead of the Copper/Stainless Steel #409/Copper cores. This will provide a much better CTE match to the low expansion (~ 5ppm/°C) insulating glass. During this past quarter, orders were placed for sheets of Copper/Molybdenum/Copper, but only began to arrive on March 14.
- Begin work with 40 mil thick metal core
- Investigate Center Conductor printing and/or plating
- Begin Thermal Cycle Testing (-40°C to +150°C)

I. References

(1) Gutierrez, C. P., Mosely, J. R and Wallace, T. C., *J.Electrochem Soc* , **109,** 923 (1962).

(2) Sussman, A, and Ward, T, *RCA Rev* , **42,** 178, (1981).

(3) Stots, S, *J. Colloid and Interfacial Sci.* , **65**, 118 (1978).

(4) Hang, K. and Andrus, James U.S. Patent #4376031, 3/31/82. "Apparatus for Electrophoretic Deposition."

Section II
WBS Task 1.2 : LTCC Ceramic Development

A. Task Objective

The development of suitable ceramic compositions for use as an inter-layer dielectric of a substrate having high density multilayer wiring. The ceramic will be processed into a green tape for the fabrication of high reliability modules using low cost processing techniques.

B. Introduction

The development of suitable ceramic compositions for use as an inter-layer dielectric in the multilayer wiring structure of the substrate is one of the principal tasks of the project. The physical, thermal and dielectric properties required of this material makes its development a major challenge as well. We have begun a systematic effort to prepare and evaluate potential dielectric compositions. A brief description of this work and the progress made to-date is given below.

The required attributes for the dielectric material are listed in Table II.1. Of these, co-sinterability with silver conductors and thermal expansion matching to the Cu/Mo/Cu core are essential for the fabrication of the low temperature cofired ceramic on metal (LTCC-M) structure. The dielectric characteristics (dielectric constant and loss) are determined by the need to make the module useful for high frequency applications. Both are required to be as low as possible. In addition, since the bonding terminals on the surface of the substrate have to be plated with nickel and gold, the dielectric material should be resistant to leaching in the highly acidic or alkaline plating solutions used. The need for low cost is emphasized to remind ourselves to stay away from materials and methods for their preparation that are difficult or expensive, in the pursuit of the ultimate in dielectric properties (e.g. materials derived from sol-gel techniques).

Unlike in the case of free-sintered multilayer ceramic substrates, where strength of the ceramic is of primary importance in handling, assembly and use, the dielectric layers in the LTCC-M are supported on a metal base making the strength of the ceramic one of secondary importance. Since dense sintering of the ceramic dielectric is required for good surface characteristics and thickness control, the ceramic dielectrics in the LTCC-M do indeed possess reasonably good strength. The surface of the LTCC-M substrates must be flat, smooth and free of large pores in order to permit the fabrication of additional thin film, polyimide-copper wiring layers if needed.

C. Dielectric Properties

One of the principal considerations in the choice of the dielectric material for the ASEM module is its dielectric characteristics. We are seeking to develop materials that are characterized by low dielectric constants and, in particular, very low values of dielectric loss at frequencies up to about 20 GHz. Glasses and glass-ceramics in the alkali and alkaline earth aluminoslicate systems have dielectric constants below 8 and exhibit low dielectric losses in KHz frequency range. The dielectric loss spectrum of insulating materials is typified by having loss maxima such as shown schematically in Figure II.1. At frequencies in the visible and ultraviolet regions, the polarization response is mainly electronic. In the region of infrared down to microwave perturbations of the lattice vibration

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Table II.1

DIELECTRIC COMPOSITIONS

Requirements

1. Good Dielectric Characteristics (Low k, low loss)
2. Sinterability between 900 ° - 1000 °C
3. Thermal Expansion Match to Metal Core (Cu-Mo-Cu)
4. Compatibility with Silver Inks
5. Resistant to Leaching in Plating Baths
6. LOW COST

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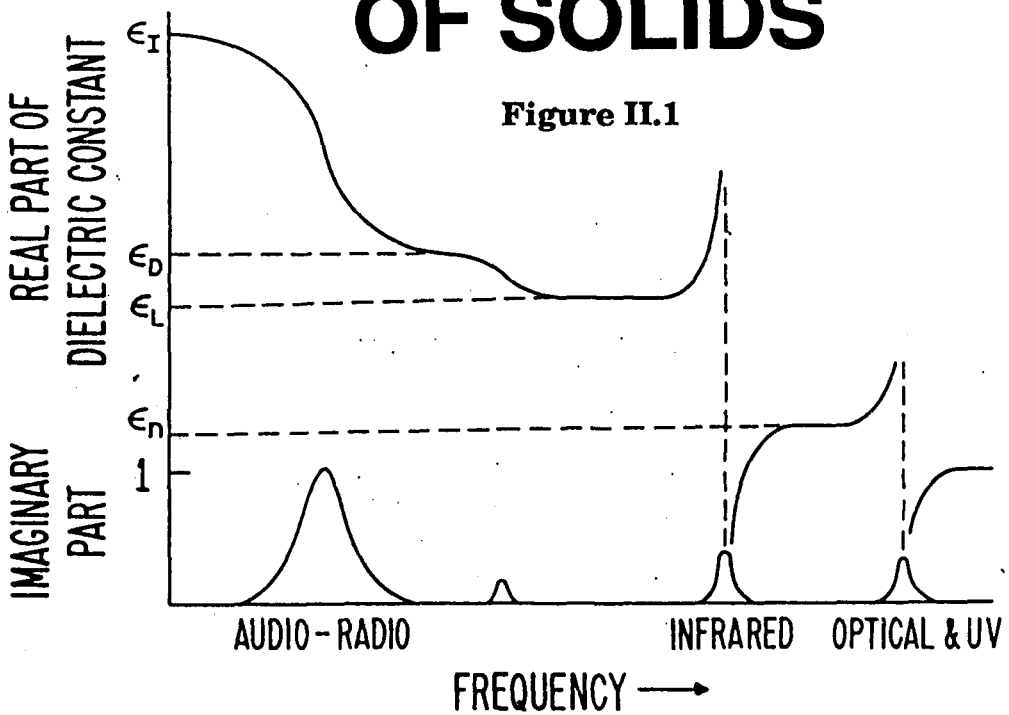
DIELECTRIC BEHAVIOR OF SOLIDS

Figure II.1



Schematic representation of the dielectric response

- ε_n **Electronic polarization**
- ε_l **Lattice polarization**
- ε_d **Dipole polarization**
- ε_i **Interfacial polarization**

modes are superimposed on the electronic polarization response. In the radio and the audio range, orientation of lattice dipoles, point defects or dipolar ions situated in lattice or interstitial sites, contributes to the polarization. Finally, at still lower frequencies, interfacial polarization predominates the total dielectric response

Dielectric properties of some oxides and glasses over a wide frequency regime are shown in Figures II.2 and II.3. Steatite and sapphire are found to posses some of the lowest values for dielectric loss (below 0.002) over the entire frequency range. Other ceramic materials in this category are BeO, fosterite ($MgOSiO_2$), and cordierite. Among the glasses, fused silica has the lowest dielectric loss throughout the frequency spectrum. Other binary and ternary silicate glasses have losses in the 0.004 range, significantly higher than that of fused silica. Also, at frequencies above 10^8, the losses start to increase, doubling to 0.008 at 10^{10} hertz. It is believed that this upturn in dielectric loss is associated with the $-SiO^-$ sites created by the breakage of Si-O-Si network in the presence of network modifiers such as alkali and alkaline earth ions.

D. Glass-ceramic Materials

The need for co-sinterability with silver thick film inks requires that the chosen composition be such that it can sinter to a dense body at temperatures in the range of 700 - 900°C. Invariably, such compositions fall into two categories viz. devitrifying glasses and mixtures of glass and ceramics. The former yield glass-ceramics, highly crystalline bodies characterized by very fine microstructure and low residual glass content distributed at the interstices amongst the crystallites. The properties of the glass-ceramics are mainly determined by those of the crystalline species formed, and are often quite different from those of the parent glass.

In case of compositions comprising the mixtures of a glass and a crystalline compound, the resulting structures are often termed as glass+ceramic or as glass-bonded ceramic. Their microstructures are characterized by ceramic grains completely surrounded by a glassy matrix, with or without a reaction layer between the two. Often the reaction layer gives rise to new crystalline species. The viscosity characteristics of the glass determines the sintering temperature for the dielectric system, and the properties of the resulting ceramic are often predictable from those of the constituents on the basis of either additive or logarithmic mixing rules applicable to simple mechanical mixtures. Any new interfacial reaction product between the glass and the ceramic grains can greatly modify the properties of the resulting ceramic body.

We are exploring both of the above approaches for developing the dielectric for the ASEM module.

(a) Sinterable glass-ceramics:

The first step is to select a glass composition based on the desired crystalline phase expected to yield a glass-ceramic with the required dielectric properties and thermal expansion coefficient. If the initial composition prepared approaches these properties and, in addition, is sinterable in the required temperature range, the next step is to tailor the composition by making small variations in the proportions of the constituents, to improve sinterability, to adjust the thermal expansion coefficient, and to improve the dielectric behavior.

Figure II.2

DIELECTRIC PROPERTIES
1. Ceramics

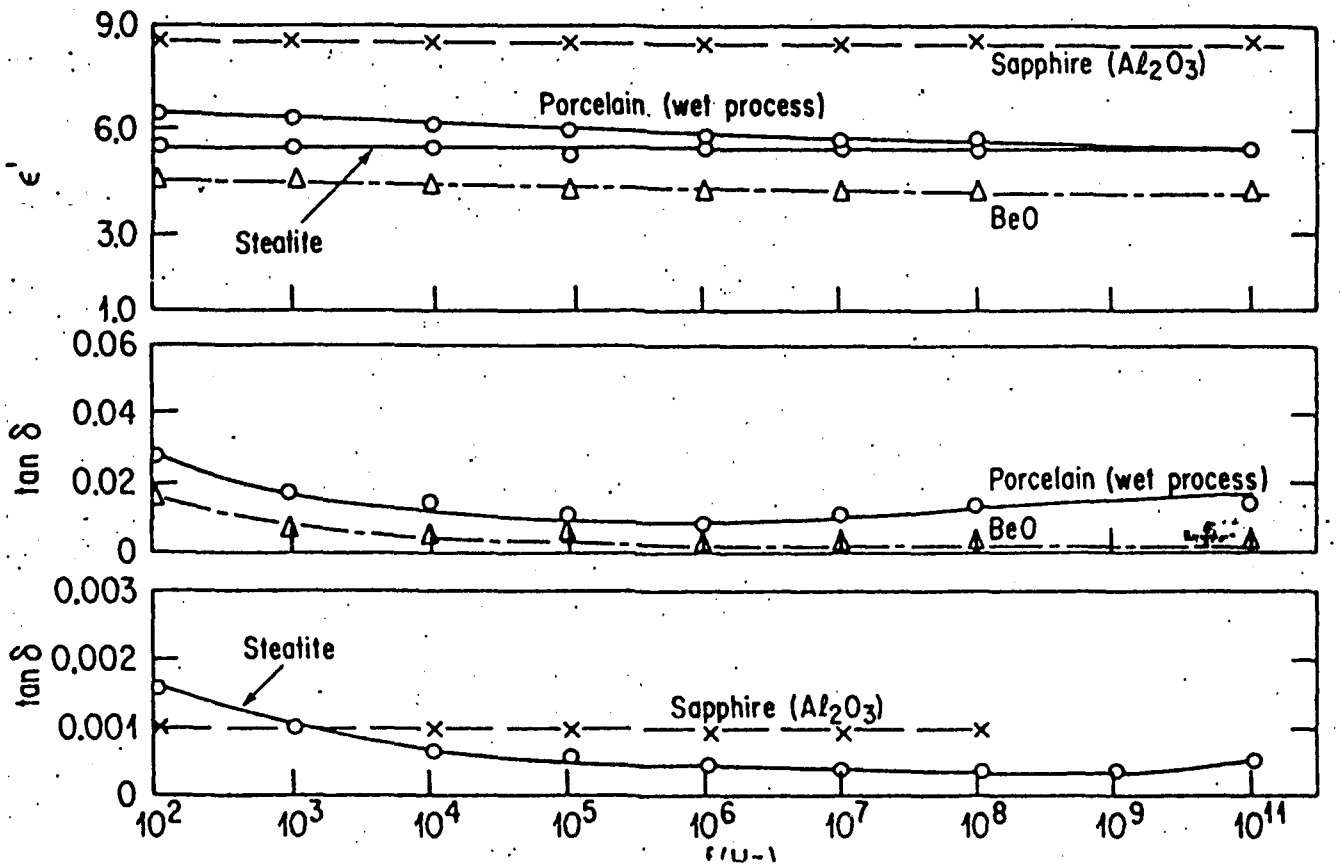
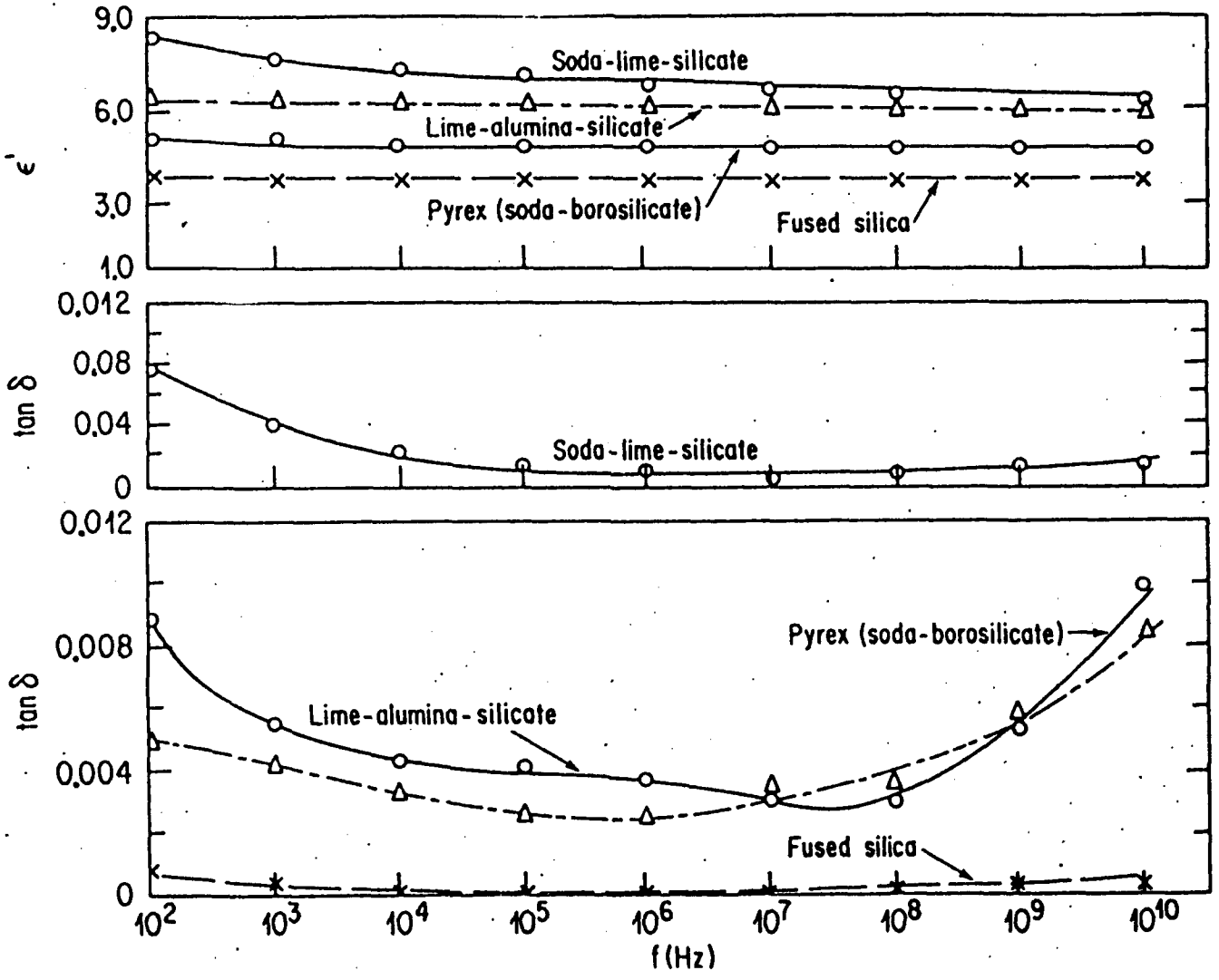


Figure II.3

DIELECTRIC PROPERTIES
2. Glasses



Several alkali and alkaline earth aluminosiliate glasses in the systems shown below, have been melted. These glasses are being evaluated in the manner shown in Figure II.4, designed to weed out unsuitable glass compositions early in the evaluation cycle.

Glass-ceramic Systems Under Evaluation

Calcium - alumino-silicate (anorthite)
Zinc-alumino-silicate
Lithium-alumino-silicate (spodumene)
Magnesium-alumino-silicate (cordierite)
Barium-alumino-silicate
MgO-Al_2O_3-PbO-SiO_2

(b) Glass+Ceramic Systems:

We are evaluating systems using a commercial borosilicate glass known to possess the desired sintering characteristics and possessing a low dielectric constant and dissipation factor as the matrix glass. The ceramic fillers are chosen for their ability to prevent excessive viscous flow during sintering, and to modify the thermal expansion of the resulting body to match that of the metal base (Cu/Mo/Cu). A further important consideration in the choice of the filler is that it should possess very low dielectric loss characteristics at high frequencies. Among such fillers are alumina, beryllia, steatite, cordierite, quartz or fused silica, and fosterite. The ceramic composition may also contain one or more other ingredients, ceramic or glass, to further improve the thermal expansion, *sinterability* and adhesion to the base metal.

Our initial evaluations have begun on compositions based on mixtures of borosilicate glass with either steatite or fosterite as the filler.

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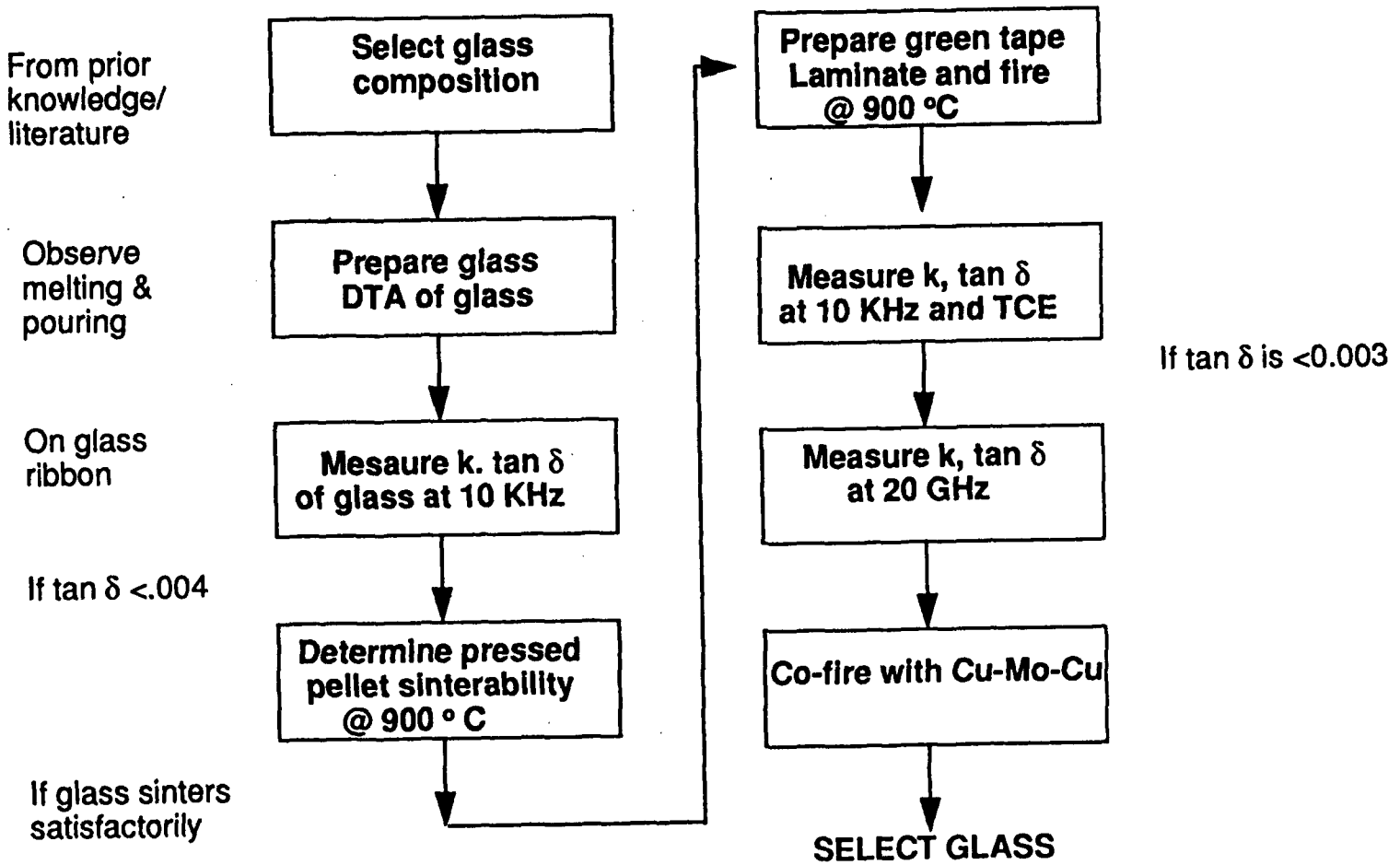
Figure II.4

DIELECTRIC COMPOSITIONS
Evaluation Procedure



E. Results to Date

We have now identified several glass-ceramic compositions and glass +ceramic mixtures having (i) sinterability at about 900 C, (ii) thermal expansion coefficient in the range of 4.5 - 6.2 ppm/°C (TCE of Cu/Mo/Cu ranges from 5.5 - 6.2ppm/°C depending on the ratio of copper to molybdenum thicknesses). Figure II.5 and II.6 show the DTA and thermal expansivity plots for one such dielectric glass composition. The dielectric properties of these compositions have been determined at 10 KHz using a capacitance bridge and at about 20 GHz using a Dielectrometer. These data are shown in Table II.2 and Figure II.7. From these, there appear to be several potential candidate dielectric compositions for the ASEM module with acceptable loss characteristics.

Table II: Dielectric Loss Data for LTCC Compositions

Glass	Dielectric Const. (15 - 20 GHz)	Loss (15 - 20 GHz)	Loss (10 KHz)
#1	3.8	0.002	
#2	3.8	0.0045	0.001
#3	6.6	0.007	0.001
#4	4.9	0.004	0.001
#5	4.8	0.005	
#6	4.3	0.003	
#7	7.1	0.0075	
#8	4.8	0.015	0.0120
#9	3.9	0.002	
#10	4.8	0.006	0.003
#11	4.2	0.004	
#12	3.6	0.004	0.001
#13	4.7	0.002	0.001
#14	5.3	0.009	0.003
#15	4.3	0.003	0.002
#16	4.2	0.004	0.001
#17	5.6	0.003	0.002
#18	4.5	0.0015	0.0015

Sample: KU-4 GLASS POWDER
Size: 30.0000 mg
Method: 10°C/MIN TO 1000°C
Comment: STATIC

DTA

File: C:KU4GLASSDT.01
Operator: K. PALIT
Run Date: 17-Feb-94 14:05

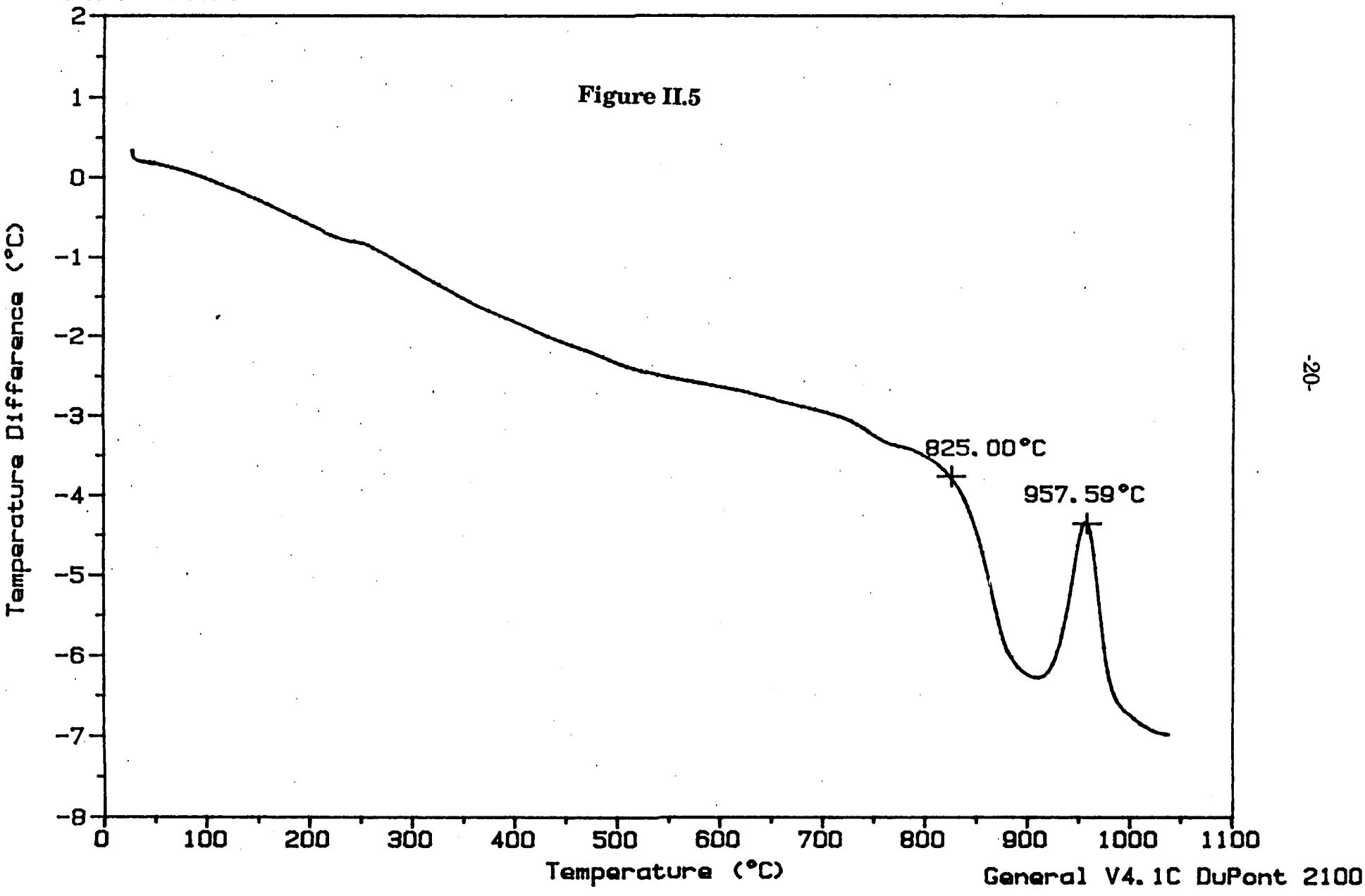


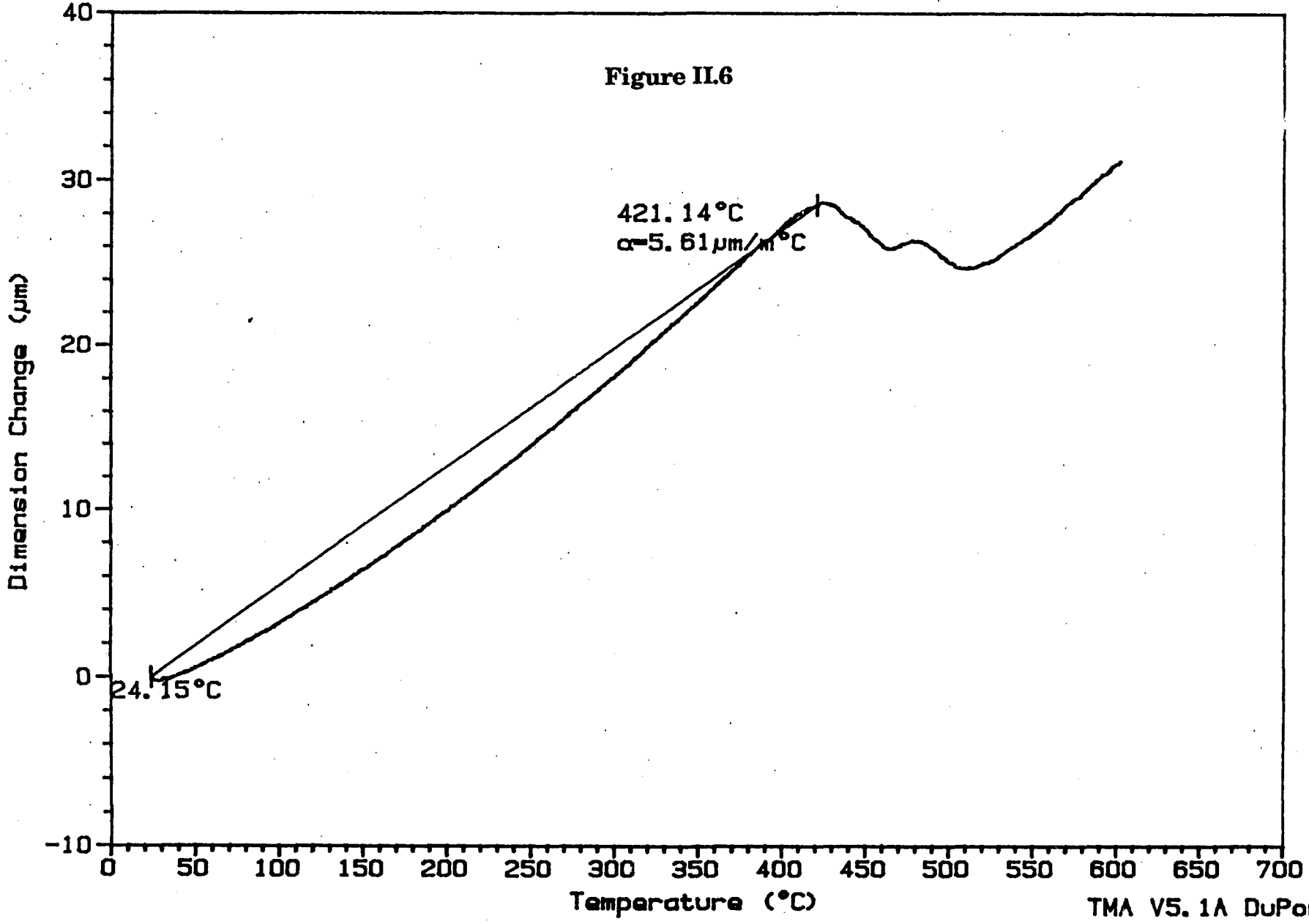
Figure II.5

Sample: KU-4 GLASS
Size: 12.8000 mm
Method: 6°C/MIN TO 600°C
Comment: STATIC

TMA

File: C:KU4TMA.01
Operator: K. PALIT
Run Date: 21-Feb-94 09:29

Figure II.6



TMA V5.1A DuPont 2100

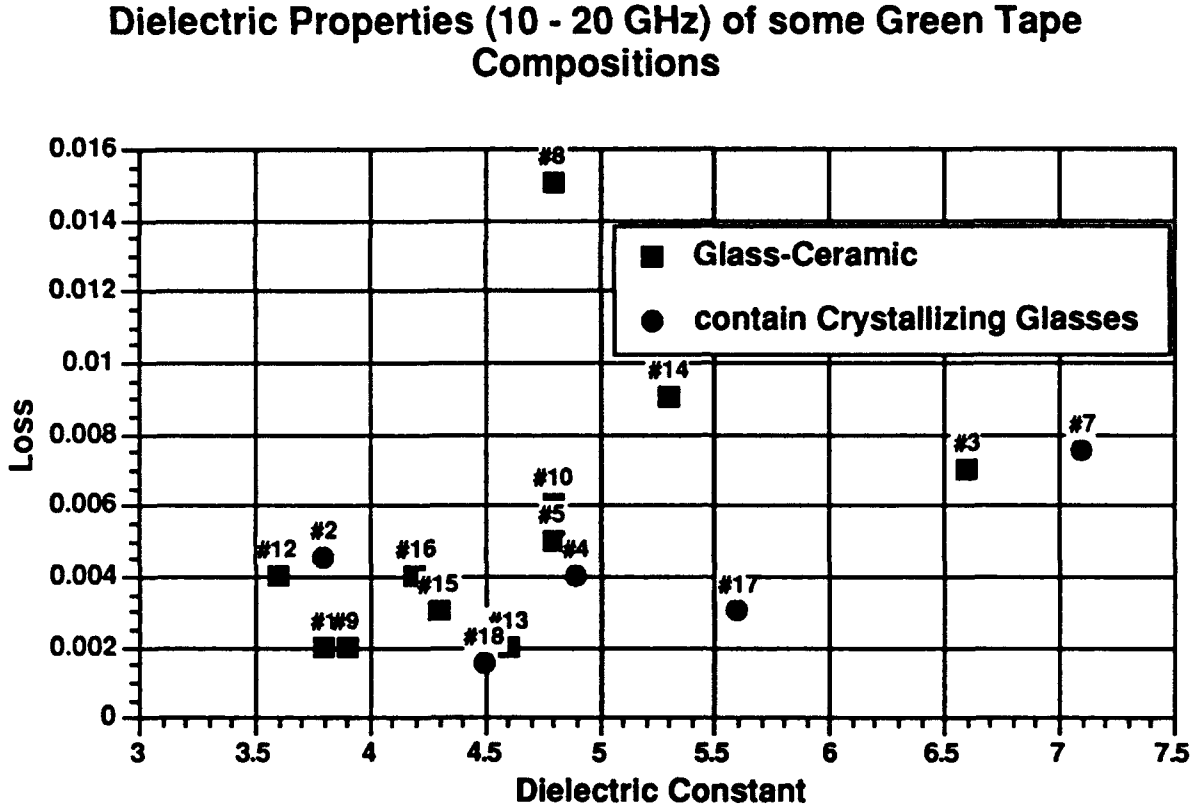


Figure II.7: Dielectric data at microwave frequencies for LTCC ceramic compositions

F. Important Findings and Conclusions

Several ceramic formulations have been developed this past quarter that exhibit excellent high frequency dielectric properties and have a CTE that is between Si and GaAs. These formulations show promise for use as the basis of the green tape that will form the LTCC-M structure.

G. Plan for the Upcoming Quarter

The emphasis next quarter will concentrate on completing the evaluation of candidate materials and choosing a ceramic composition for the green tape formulation. The major activities that will take place during this period are listed below:

1. Compilation of dielectric characterization of leading candidate compositions
2. Measure CTE of the glass-ceramics and compare to that of Cu/Mo/Cu
3. Detailed characterization of the sintering behavior of the glasses
4. Cofiring with silver conductors to assess compatibility with silver
5. Determine the chemical resistance of the dielectric to plating baths
6. Green tape formulation for the chosen dielectric material
7. Preliminary experiments of firing onto Cu/Mo/Cu base plates to evaluate glaze material and bonding process and camber issues.
8. Lamination process optimization

Section III
WBS Task 1.4: Thin Film Interconnect Structure Integration

A. Task Objective

The objective of this part of the program is to demonstrate that polyimide-copper interconnect structures can be built on top of the ASEM ceramic substrate. This will be accomplished by the actual fabrication of a multi-level, thin film interconnect structure on the final ASEM test vehicle and subjecting this structure to the relevant reliability tests.

B. Introduction

Two key substrate attributes necessary for thin film processing are (i) very good flatness and (ii) very high degree of surface smoothness. The first attribute critically depends on obtaining a good thermal expansion match between the substrate and the metal core so that camber-free substrates can be obtained even in unbalanced, double-sided LTCC-M substrates. In all likelihood, the desirable surface smoothness for thin film fabrication can only be obtained after lapping and polishing. Substrate camber again becomes important because it will determine the ease of lapping and polishing. It is also important that the substrate dielectric sinters dense with a minimum of porosity because pores, especially large ones, introduce defects in the thin film interconnect structures. Well distributed fine porosity can be tolerated to some extent.

In preparation for building the test thin film structure on the ASEM test vehicle, our current activity in this area is aimed at acquiring familiarity with the some of the important elements of thin film interconnect fabrication methods. We have chosen to do this by building some test structures on polished alumina substrates using available masks. Once these skills in processes and materials are acquired, more elaborate multilevel test structures will be constructed to enable assessing process yields and other issues. Masks for such structures are being designed.

Two generic approaches to thin film interconnect fabrication are being practiced now. One of the processes will utilize a photo-imaginable polyimide and other a non-photosensitive polyimide. The process that is easiest to practice will be chosen for the ASEM test vehicle

C. Results to Date

We have so far constructed patterned metal and patterned polyimide structures on alumina substrates, examples are shown in Figures III.1 and III.2. In building these structures, the following processing steps were practiced:

Substrate planarization by lapping and polishing
Seed layer (Cr-Cu) sputtering
Photoresist patterning
Electroplating of copper , nickel and gold in patterned resist
Selective electroless plating of nickel
Polyimide spinning and curing
Photosensitive polyimide exposing and developing
Ion -beam subtractive etching
Wet chemical sub-etching

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THIN FILM PROCESS

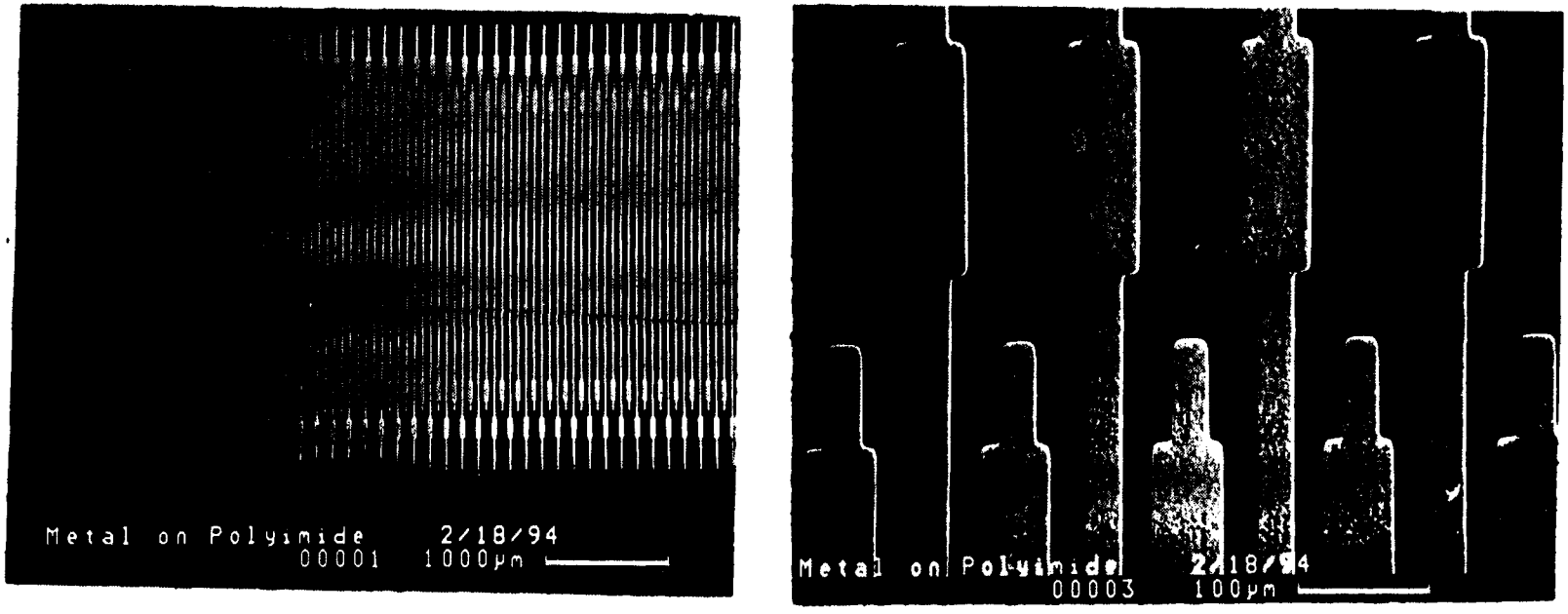

Figure III.1

SEM of circuit features of Cu-Ni-Au elctroplated through photoresist

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THIN FILM PROCESS

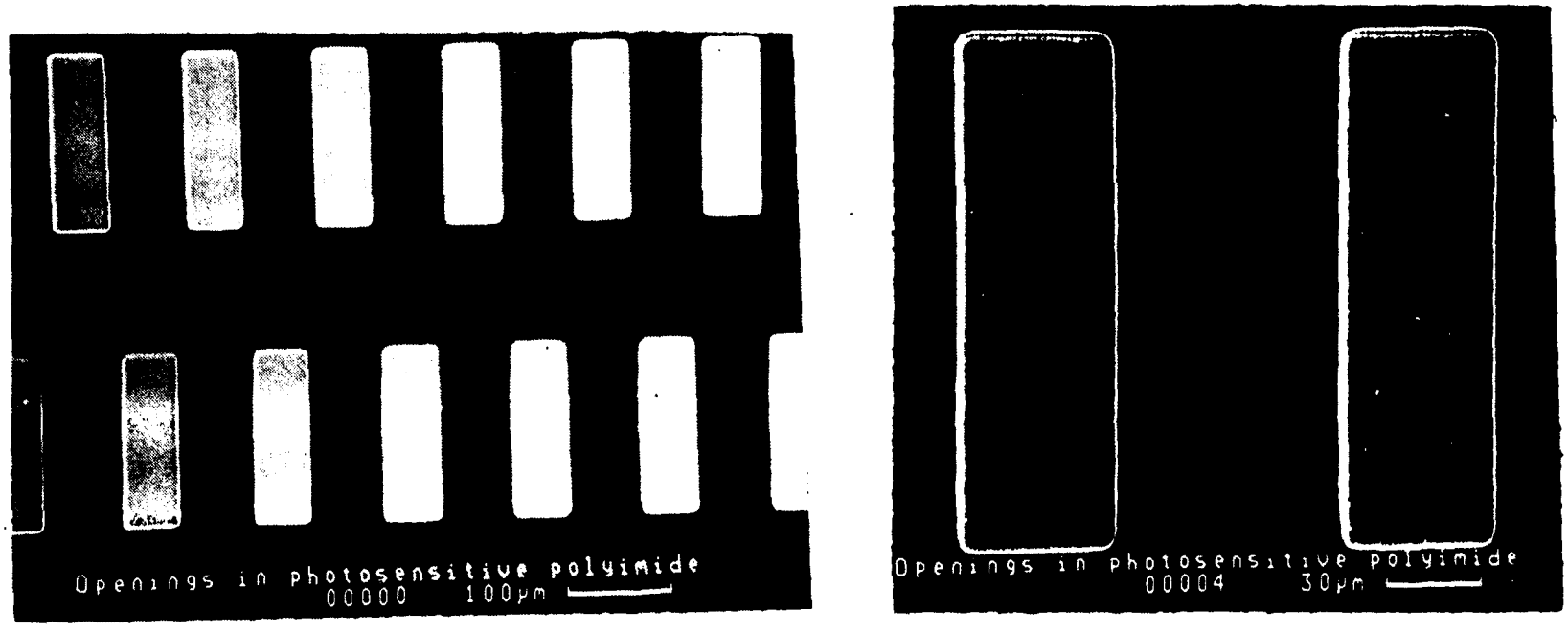

Figure III.2

SEM of Openings in CG-412 Photosensitive Polyimide

D. Plan for the Upcoming Quarter

During the next reporting period the polyimide thin film interconnect fabrication elements will be integrated to fabricate a two level, testable interconnect structure on polished alumina substrates. During this period we will also examine to see if there are any unique considerations to practice the same process on the chosen LTCC-M substrates. Furthermore, we will explore extending the thin film interconnect processing to use the BCB materials manufactured by Dow Chemical as the inter-layer dielectric.

Some specific tasks that will be carried out during this period are the following:

- Process optimization for via hole (≤2 mil diameter) in photosensitive polyimide.
- Process for thin nickel protection layer coating over conductor features by electroless plating.
- Mask design and acquisition for two layer test pattern
- Evaluation of process using non-photosensitive polyimides manufactured by DuPont.
- Start fabrication of two level test structures using one of the thin film processes.
- Explore the possibility of using BCB dielectric layers.

Section IV
Important Findings

Electrical Feedthroughs in Metal Core

A limited number of electrical feedthroughs have been fabricated in 13 mil diameter holes in a 20 mil thick metal core, using screen printing techniques. This technique shows promise as a low cost, mass fabrication process for producing a large number of electrical feedthroughs. A glass (for the feedthrough insulator) has been found that exhibits good adhesion and wetting of the metal core surface. Furthermore, it is thought that these techniques can be extended to produce 50Ω interconnections (20 - 30 mil diameter).

LTCC Ceramic Development

Several ceramic formulations have been developed this past quarter that exhibit excellent high frequency dielectric properties and have a CTE that is between Si and GaAs. These formulations show promise for use as the basis of the green tape that will form the LTCC-M structure.

Section V
Significant Developments

Several of the LTCC ceramics that have been developed show low dielectric loss ($0.001 < \tan \delta < 0.002$) in the 10 - 20GHz frequency range. Such ceramics are highly desirable for the construction of military T/R modules. Developing these ceramics into an LTCC-M process technology will show a path to the production of high volume, low cost T/R modules for military electronics.

Section IV
Plan for Further Research

The major emphasis of the research program will be on the metal core through-hole fabrication process.

Metal Core Fabrication

- The screen printing techniques, which do not suffer from the shielding limitations of electrophoresis, will be emphasized during the upcoming quarter. The techniques will be optimized for uniform coating of the insulating glass within the holes.
- Through-holes will be fabricated in Copper/Molybdenum/Copper cores instead of the Copper/Stainless Steel #409/Copper cores. This will provide a much better CTE match to the low expansion (~ 5ppm/°C) insulating glass. During this past quarter, orders were placed for Copper/Molybdenum/Copper sheets, but they only began to arrive on March 14.
- Investigate Center Conductor printing and/or plating
- Begin work with 40 mil thick metal core
- Begin Thermal Cycle Testing (-40°C to +150°C)

LTCC Ceramic Development

The emphasis next quarter will concentrate on completing the evaluation of candidate materials and choosing a ceramic composition for the green tape formulation. The major activities that will take place during this period are listed below:

1. Compilation of dielectric characterization of leading candidate compositions
2. Measure CTE of the glass-ceramics and compare to that of Cu/Mo/Cu
3. Detailed characterization of the sintering behavior of the glasses
4. Cofiring with silver conductors to assess compatibility with silver
5. Determine the chemical resistance of the dielectric to plating baths
6. Formulate green tape for the chosen dielectric material
7. Perform preliminary experiments of firing onto Cu/Mo/Cu base plates to evaluate glaze material, bonding process, and camber issues.
8. Lamination process optimization

Thin Film Interconnect Structure Integration

During the next reporting period the polyimide thin film interconnect fabrication elements will be integrated to fabricate a two-level, testable interconnect structure on polished alumina substrates. During this period we will also examine to see if there are any unique considerations to practice the same process on the chosen LTCC-M substrates. Furthermore, we will explore extending the thin film interconnect processing to use the BCB materials manufactured by Dow Chemical as the inter-layer dielectric.

Some specific tasks that will be carried out during this period are the following:

- Process optimization for via hole (≤2 mil diameter) in photosensitive polyimide.
- Process for thin nickel protection layer coating over conductor features by electroless plating.

- Mask design and acquisition for two layer test pattern
- Evaluation of a process using non-photosensitive polyimides manufactured by DuPont.
- Start fabrication of two level test structures using one of the thin film processes.
- Explore the possibility of using BCB dielectric layers.

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The quarterly progress for the Ceramic/Metal Composite Circuit-Board-Level Technology for Application Specific Electronic Modules is described in this report. Data is reported for the following tasks: Metal Core Fabrication, LTCC Ceramic Development, and Thin Film Interconnect Structure Integration

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